

# Power Amplifier, 40 dBm, 10 W 37 - 43 GHz



CGY2651UH/C1

Rev. V1

## Features

- Gain: 18 dB
- Output Power: 40 dBm @ 40 GHz
- PAE: 30 %
- Power Supply: 12 V, 0.84 A
- 50  $\Omega$  Input & Output Matched
- Chip Size: 3.6 x 2.8 mm
- Tested Inspected Known Good Die (KGD)
- Demonstration Boards Available
- Space and MIL-STD Available
- RoHS\* Compliant

## Applications

- Radar
- Telecommunication
- Spatial

## Description

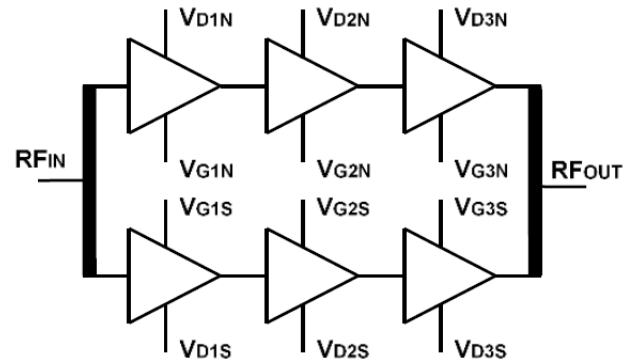
The CGY2651UH/C1 is a high-performance GaN Power Amplifier MMIC designed to operate in the Ka-band.

The CGY2651UH/C1 has 40 dBm of output power and 30% PAE @ Psat & 40 GHz.

The performances of the CGY2651UH/C1 make it well suited to be used in Radar, Telecommunication and Space applications.

This technology is being evaluated for space applications.

## Block Diagram



## Ordering Information

Part Number	Package
CGY2651UH/C1	DIE

\* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

**Electrical Specifications: Measured On Wafer, Freq. = 37 - 43 GHz, T<sub>A</sub> = +25°C**

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Drain Supply Voltage	—	V	—	12	—
Total Supply Current	@ P <sub>SAT</sub>	A	—	2.7	—
Gain	—	dB	—	18	—
Saturated Power (P <sub>SAT</sub> )	—	dBm	—	41	—
Power Added Efficiency	PAE @ 30 GHz	%	—	30.5	—
Output IP3	—	dBm	—	TBD	—
Input Return Loss	@ 50 Ω	dB	—	8	—
Output Return Loss	@ 50 Ω	dB	—	10	—

**Absolute Maximum Ratings<sup>1,2</sup>**

Parameter	Absolute Maximum
Input Power	25 dBm
Voltage Gate Drain	-2.5 V to 0 V 10 to 15 V
Current Gate Drain	-10 to +10 mA 450, 900, 1800 mA
Junction Temperature	+200°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +85°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

**Thermal Characteristics**

Parameter	Absolute Maximum
Thermal Resistance @+ 25°C @ +60°C	3.25° C/W 4.78° C/W

**Handling Procedures**

Please observe the following precautions to avoid damage:

**Static Sensitivity**

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

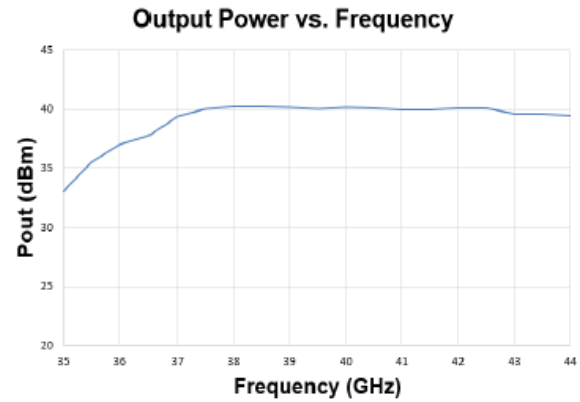
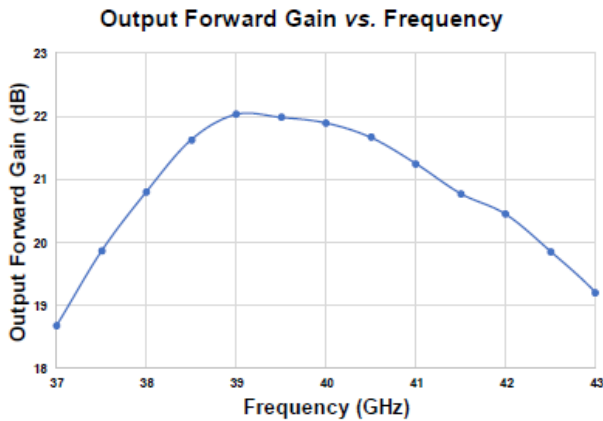
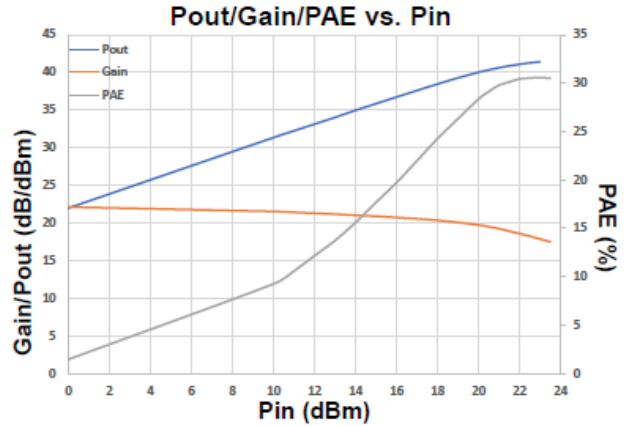
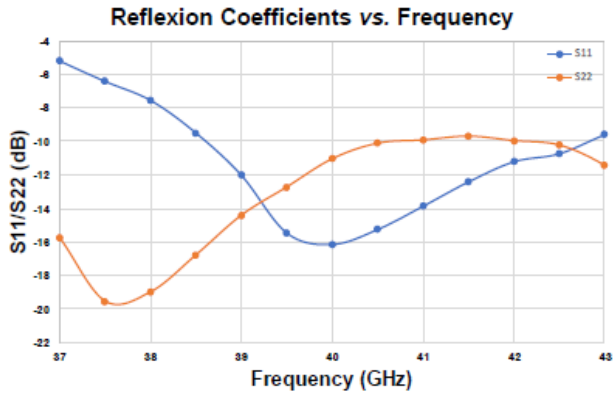
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## Typical Performance Curves: On Wafer Measurements

TA = + 25°C, VD1 = VD2 = VD3 = 12 V; ID1 = 120 mA; ID2 = 240 mA; ID3 = 480 mA

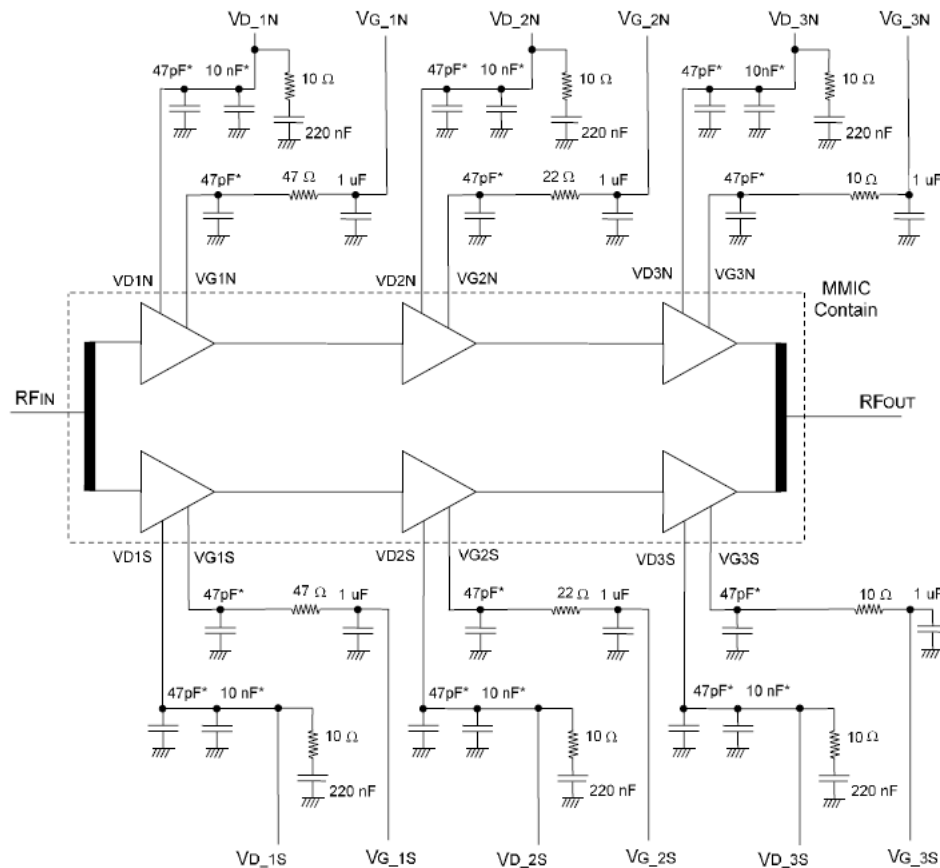


**Application Schematic**

Decoupling scheme depends on customer implementation, in order to prevent instability it is highly recommended to place a 47pF RF decoupling chip capacitor at each DC terminal with the shortest possible bonding wires. Additionally, a 10nF chip capacitor can be added on the drain 3 connection.

The decoupling network depends on supply, on grounding environment, on form factor, on all parasitics added by the customer environment. According to this, the appropriate network sometimes need to be fine-tuned in accordance with rules applicable in the high frequency domain.

It may also be required to add very low frequency, high capacitor value. On each drain a 10 Ohms / 10 nF RC series network made of 0402 format capacitors have been implemented on the reference test-jig.

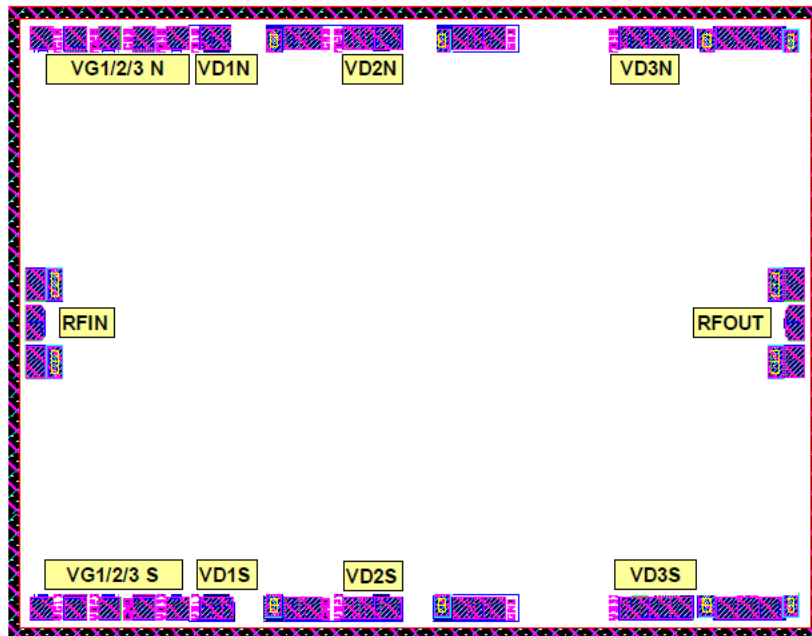


Component Name	Value	Type	Comment

### Pad Layout

The Die is symmetrical on the RF axis. The die positioned top view with RF input on the left and RF output on the right show DC accesses on the top labelled north (N) and DC accesses on the bottom labelled south (S).

VD1N, VD2N, VD3N, VG1N, VG2N, VG3N are DC signals applied on the north side while VD1S, VD2S, VD3S, VG1S, VG2S, VG3S are DC signals applied on the south side. Many ground accesses are complementing the pad layout. The backside is the ground reference plan.



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